IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 1-5 and 8-12 in accordance with the following:

1. (Currently Amended) A memory control circuit comprising:

a write error protect circuit, including

a register,

a first gate that sets one of a first data and a second data supplied from the outside into the register, and

a second gate that disables output of a write signal supplied from the outside to a memory ~~by resetting a~~ when the register is reset, outputs the write signal ~~supplied from the outside~~ to the memory ~~upon writing a~~ when the first data is set into the register, and prevents the output of the write signal to the memory ~~upon writing a~~ when the second data ~~that is different from the first data~~ is set into the register.

2. (Currently Amended) The memory control circuit according to claim 1, wherein the ~~write error protect circuit includes~~register comprises:

a first latch circuit that stores "0" by reset; and

a second latch circuit that stores "1" by reset, to which an output signal from the first latch circuit is input;

~~a~~wherein the first gate ~~that~~ outputs ~~a register setting data supplied from the outside~~ one of the first data and the second data to the first latch circuit when an output signal from the second latch circuit is "1", and outputs "0" to the first latch circuit when the output signal from the second latch circuit is "0";, and ~~a~~the second gate ~~that~~ outputs ~~a~~the write signal ~~supplied from the outside~~ to the memory only when the output signal from the first latch circuit is "1".

3. (Currently Amended) A memory device comprising:

a memory that is rewritable by an input of a write signal from outside to the memory; and

a memory control circuit ~~including~~that includes a write error protect circuit including

a register,

a first gate that sets one of a first data and a second data supplied from outside into the register, and

a second gate that disables output of the write signal to the memory ~~by resetting a~~ when the register is reset, outputs the write signal to the memory ~~upon writing a~~ when the first data is set into the register, and prevents the output of the write signal to the memory ~~upon writing a~~ when the second data ~~that is different from the first data~~is set into the register.

4. (Currently Amended) The memory device according to claim 3, wherein the ~~write error protect circuit~~register comprises:

a first latch circuit that stores "0" by reset; and

a second latch circuit that stores "1" by reset, to which an output signal from the first latch circuit is input~~;~~,

~~a~~wherein the first gate ~~that~~ outputs ~~a register setting data supplied from the outside~~one of the first data and the second data to the first latch circuit when an output signal from the second latch circuit is "1", and outputs "0" to the first latch circuit when the output signal from the second latch circuit is "0"~~;~~, and ~~a~~the second gate ~~that~~ outputs ~~a~~the write signal ~~supplied from the outside~~ to the memory only when the output signal from the first latch circuit is "1".

5. (Currently Amended) The memory device according to claim 3, wherein the memory is divided into a plurality of areas in which write disable, write enable, and write error protect are set independently~~;~~, and the memory includes the write error protect circuit for each area.

6. (Original) The memory device according to claim 3, wherein the memory is a nonvolatile memory.

7. (Original) The memory device according to claim 6, wherein the nonvolatile memory is a flash memory.

8. (Currently Amended) A microcomputer comprising:

a central processing unit;

a memory that is rewritable by an input of a write signal from the central processing unit to the memory; and

a memory control circuit ~~including~~that includes a write error protect circuit including

a register,

a first gate that sets one of a first data and a second data supplied from outside into the register, and

a second gate that disables output of the write signal to the memory ~~by resetting a~~ when the register is reset, outputs the write signal to the memory ~~upon writing a~~ when the first data is set into the register, and prevents the output of the write signal to the memory ~~upon writing a~~ when the second data ~~that is different from the first data~~is set into the register.

9. (Currently Amended) The microcomputer according to claim 8, wherein the ~~write error protect circuit~~register comprises:

a first latch circuit that stores "0" by reset; and

a second latch circuit that stores "1" by reset, to which an output signal from the first latch circuit is input;

~~a~~wherein the first gate ~~that~~ outputs ~~a register setting data supplied from the outside~~one of the first data and the second data to the first latch circuit when an output signal from the second latch circuit is "1", and outputs "0" to the first latch circuit when the output signal from the second latch circuit is "0";, and ~~a~~the second gate ~~that~~ outputs ~~a~~the write signal ~~supplied from the outside~~ to the memory only when the output signal from the first latch circuit is "1".

10. (Currently Amended) The microcomputer according to claim 8, wherein the memory is divided into a plurality of areas in which write disable, write enable, and write error protect are set independently;, and the memory includes the write error protect circuit for each area.

11. (Currently Amended) The ~~memory device~~microcomputer according to claim 8, wherein the memory is a nonvolatile memory.

12. (Currently Amended) The ~~memory device~~microcomputer according to claim 11, wherein the nonvolatile memory is a flash memory.

13. (Original) The microcomputer according to claim 8, wherein the central processing unit, the memory, and the memory control circuit are integrated in a same semiconductor chip.